CLAIMS

What is claimed is:

1. A method of channel bonding a plurality of multi-gigabit transceivers, the method comprises:

receiving, by a master transceiver of the plurality of multi-gigabit transceivers, a channel bonding sequence;

generating, by the master transceiver, a channel bonding request in response to the channel bonding sequence;

transmitting, by the master transceiver, the channel bonding request and channel bonding configuration information to slave transceivers of the plurality of multi-gigabit transceivers;

receiving, by each of the slave transceivers, the channel bonding sequence;

receiving, by each of the slave transceivers, the channel bonding request and the channel bonding configuration information;

processing, by each of the slave transceivers, the channel bonding request and the channel bonding sequence in accordance with the channel bonding configuration information to determine individual slave channel bonding start information;

processing, by the master transceiver, the channel bonding sequence in accordance with the channel bonding configuration information and the channel bonding request to determine master channel bonding start information; and

commencing channel bond writing of respective data to and reading of the respective data from corresponding buffers by the master transceiver and the slave transceivers in

accordance with the individual slave channel bonding start information and the master channel bonding start information.

2. The method of claim 1, wherein the receiving the channel bonding sequence by the master transceiver further comprises:

receiving the channel bonding sequence within incoming data; and

detecting the channel bonding sequence within the incoming data.

3. The method of claim 1 further comprises:
designating one of the plurality of multi-gigabit transceivers as the master transceiver; and

designating at least some of remaining ones of the plurality of multi-gigabit transceivers as the slave transceivers.

4. The method of claim 1, wherein the receiving the channel bonding sequence by each of the slave transceivers further comprises:

receiving the channel bonding sequence within incoming data; and

detecting the channel bonding sequence within the incoming data.

5. The method of claim 1, wherein the receiving, by each of the slave transceivers, the channel bonding request and the channel bonding configuration information further comprises:

receiving the channel bonding request and the channel bonding configuration information from the master transceiver; or

receiving the channel bonding request and the channel bonding configuration information from at least one intervening slave transceiver.

6. The method of claim 1 further comprises the master transceiver generating the channel bonding configuration information further to include:

a number of slave transceivers;

propagation delays of each of the slave transceivers with respect to the master transceiver transmitting the channel bonding request; and

clock correction information.

7. The method of claim 6, wherein the generating the clock correction information comprises:

generating pointer separation information;

generating an address offset; and

generating an adjust enable signal.

8. The method of claim 7, wherein the generating the pointer separation comprises:

determining a read pointer of the master transceiver when the channel bonding sequence is received to produce a master read pointer;

determining a write pointer of the master transceiver when the channel bonding sequence is received to produce a master write pointer; and

determining the pointer separation as a difference between the master read pointer and the master write pointer.

9. The method of claim 7, wherein the generating the address offset comprises:

determining byte positioning of the channel bonding sequence with respect to a word line of memory of the master transceiver; and

establishing the address offset based on the byte positioning.

10. The method of claim 7, wherein the processing, by each of the slave transceivers, the channel bonding request and the channel bonding sequence in accordance with the channel bonding configuration information to determine individual slave channel bonding start information comprises:

delaying the channel bonding sequence for a predetermined period of time based on the propagation delays of a corresponding one of the slave transceivers to produce a delayed channel bonding sequence;

determining whether receipt of the channel bonding request and the delayed channel bonding sequence are within a time window;

when the receipt of the channel bonding request and the delayed channel bonding sequence are within the time window:

determining a unique hold time based on a difference between the propagation delay of the corresponding one of the slave transceivers and a maximum propagation delay;

storing an address at which the channel bonding sequence was received by the corresponding one of the slave transceivers to produce a channel bonding sequence address;

determining a channel bonding write start address based on at least one of: the channel bonding sequence address, the channel bonding request, and the unique hold time; and

adjusting a read pointer and a write pointer of the corresponding one of the slave transceivers based on the pointer separation, the address offset, and the channel bonding write start address.

11. The method of claim 10, wherein the determining whether receipt of the channel bonding request and the delayed channel bonding sequence are within the time window comprises:

when one of the delay channel bonding sequence or the channel bonding request is received, initiating the time window; and

determining whether the other one of the delay channel bonding sequence or the channel bonding request is received prior to expiration of the time window.

12. The method of claim 10, wherein the adjusting the read pointer and the write pointer further comprises:

adding the address offset to the read pointer and to the write pointer.

13. The method of claim 1, wherein the processing of the channel bonding sequence in accordance with the channel bonding configuration information and the channel bonding request to determine master channel bonding start information comprises:

storing an address at which the channel bonding sequence was received to produce a channel bonding sequence address; and

determining a channel bonding write start address based on the channel bonding sequence address and maximum propagation delay of the channel bonding configuration information.

14. A method for channel bonding by a multi-gigabit transceiver, the method comprises:

determining whether the multi-gigabit transceiver is a master transceiver or a slave transceiver;

when the multi-gigabit transceiver is the slave transceiver:

detecting a channel bonding sequence at a given time to produce a detected channel bond sequence;

delaying the detected channel bonding sequence for a predetermined period of time to produce a delayed channel bonding sequence;

receiving a channel bonding request at a second given time;

determining whether the receiving of channel bonding request and the delayed channel bonding sequence are within a time window;

when the receiving of channel bonding request and the delayed channel bonding sequence are within the time window:

aligning data with respect to data alignment of the master transceiver to produce aligned data; and

synchronizing the aligned data with data of the master transceiver.

15. The method of claim 14, wherein the determining whether the receiving of channel bonding request and the delayed channel bonding sequence are within the time window comprises:

determining whether the delayed channel bonding sequence occurs, in time, before the receiving of the channel bonding request;

when the delayed channel bonding sequence occurs before the receiving of the channel bonding request:

initiating a first clock cycle count from the delay channel bonding sequence to establish the time window;

determining whether the channel bonding request is received before expiration of the first clock cycle count; and

when the channel bonding request is received before expiration of the first clock cycle count, determining that the receiving of channel bonding request and the delayed channel bonding sequence are within the time window;

when the delayed channel bonding sequence occurs after the receiving of the channel bonding request:

initiating a second clock cycle count from the receiving of the channel bonding request to establish the time window;

determining whether the delayed channel bonding sequence occurs before expiration of the second clock cycle count; and

when the delayed channel bonding sequence occurs before expiration of the second clock cycle count, determining that the receiving of channel bonding request and the delayed channel bonding sequence are within the time window; and

when the delayed channel bonding sequence occurs at substantially the same time as the receiving of the channel bonding request, determining that the receiving of channel bonding request and the delayed channel bonding sequence are within the time window.

16. The method of claim 14, wherein the aligning data with respect to data alignment of the master transceiver to produce aligned data comprises:

determining a unique hold time based on a difference between propagation delay of the master transceiver detecting the channel bonding sequence and the slave

transceiver receiving the channel bonding request and a maximum propagation delay;

storing an address at which the channel bonding sequence was received by the slave transceiver to produce a channel bonding sequence address; and

determining a channel bonding write start address based on at least one of: the channel bonding sequence address, the channel bonding request, and the unique hold time.

17. The method of claim 16, wherein the synchronizing the aligned data comprises:

adjusting a read pointer and a write pointer of the slave transceiver based on pointer separation, an address offset, and the channel bonding write start address, wherein the pointer separation corresponds to a difference between a master read pointer and a master write pointer of the master transceiver and wherein the address offset corresponds to byte positioning of the channel bonding sequence with respect to a word line of memory of the master transceiver.

18. The method of claim 14 further comprises, when the multi-gigabit transceiver is the master transceiver:

establishing the predetermined period of time based on propagation delay between the master transceiver detecting the channel bonding sequence and the slave transceiver receiving the channel bonding request.

19. The method of claim 18 further comprises:

storing an address at which the channel bonding sequence was received to produce a channel bonding sequence address; and

determining a channel bonding write start address based on the channel bonding sequence address and maximum propagation delay of channel bonding configuration information.

20. A channel bonding module for a multi-gigabit transceiver, the channel bonding module comprises:

channel bonding sequence comparator operably coupled to a buffer of the multi-gigabit transceiver, wherein the buffer temporarily stores received data, and wherein the channel bonding sequence comparator compares data blocks of the received data with a channel bonding sequence and, when a current data block of the data blocks of the received data substantially matches the channel bonding sequence, the channel bonding sequence comparator generates a channel bonding sequence detect signal;

pointer generation module operably coupled to generate a read pointer and a write pointer for the buffer; and

channel bonding processing module operably coupled to:

generate a channel bonding sequence address based on the write pointer and the channel bonding sequence detect signal;

generate a channel bonding start address based on the channel bonding sequence address and channel bonding configuration information;

generate a channel bonding start indication based on the channel bonding configuration information;

provide the channel bonding start address and the channel bonding start indication to the pointer generation module such that, at commencement of channel bonding, the write pointer corresponds to the channel bonding start address.

21. The channel bonding module of claim 20 further comprises:

a clock correction module operably coupled to:

generate pointer adjust information based on clock correction information, the read pointer, and the write pointer, wherein the clock correction information includes pointer separation information, an address offset, and an adjust enable signal; and

provide the pointer adjust information to the pointer generation module, wherein the pointer generation module adjusts the read pointer and write pointer prior to the commencement of the channel bonding.

22. The channel bonding module of claim 21 further comprises:

a master/slave module operably coupled to indicate whether the multi-gigabit transceiver is a master transceiver or a slave transceiver.

23. The channel bonding module of claim 22, wherein the channel bonding processing module further functions to: when the multi-gigabit transceiver is the master transceiver:

generate a channel bonding request in response to the channel bonding sequence detect signal;

provide the channel bonding request to slave transceivers;

generate the channel bonding configuration information to indicate a number of the slave transceivers, propagation delays of each of the slave transceivers with respect to the master transceiver transmitting the channel bonding request, and a maximum propagation delay;

when the multi-gigabit transceiver is the slave transceiver:

process the channel bonding request in accordance with the channel bonding sequence address and the write pointer to generate the channel bonding start address; and

process the propagation delay of the propagation delays for the slave transceiver and the maximum propagation delay to determine the channel bonding start indication.

24. The channel bonding module of claim 23, wherein, when the multi-gigabit transceiver is the slave transceiver, the channel bonding processing module further functions to process the channel bonding request in accordance with the channel bonding sequence address and the write pointer to generate the channel bonding start address by:

storing the channel bonding sequence detect signal for a predetermined period of time based on the propagation delays of a corresponding one of the slave transceivers to

produce a delayed channel bonding sequence detect;

determining whether receipt of the channel bonding request and the delayed channel bonding sequence detect are within a time window;

when the receipt of the channel bonding request and the delayed channel bonding sequence detect are within the time window, generating the channel bonding start address in accordance; and

when the receipt of the channel bonding request and the delayed channel bonding sequence detect are not within the time window, generating an channel bonding error indication.

25. The channel bonding module of claim 24, wherein the determining whether receipt of the channel bonding request and the delayed channel bonding sequence are within the time window comprises:

when one of the delay channel bonding sequence detect or the channel bonding request is received, initiating the time window; and

determining whether the other one of the delay channel bonding sequence detect or the channel bonding request is received prior to expiration of the time window.

26. The channel bonding module of claim 22, wherein the clock correction module further functions to:

when the multi-gigabit transceiver is the master transceiver:

generate the clock correction information to include pointer separation information, an address offset, and an adjust enable signal, wherein the generating the pointer separation includes:

determining a read pointer of the master transceiver when the channel bonding sequence is received to produce a master read pointer;

determining a write pointer of the master transceiver when the channel bonding sequence is received to produce a master write pointer; and

determining the pointer separation as a difference between the master read pointer and the master write pointer, and

wherein the generating the address offset includes:

determining byte positioning of the channel bonding sequence with respect to a word line of the buffer of the master transceiver; and

establishing the address offset based on the byte positioning.

27. The channel bonding module of claim 26, wherein the clock correction module further functions to:

when the multi-gigabit transceiver is the slave transceiver:

adjust a read pointer and a write pointer that correspond to the channel bonding start address based on the pointer separation and the address offset.

28. An integrated circuit comprises:

a plurality of multi-gigabit transceivers, wherein one of the plurality of multi-gigabit transceivers is designated as a master transceiver and remaining ones of the plurality of multi-gigabit transceivers are designated as slave transceivers;

the master transceiver is operably coupled to:

receive a channel bonding sequence;
generate a channel bonding request in response to the channel bonding sequence;

transmit the channel bonding request and channel bonding configuration information to the slave transceivers;

process the channel bonding sequence in accordance with the channel bonding configuration information and the channel bonding request to determine master channel bonding start information;

commence channel bond writing of respective data to and reading of the respective data from corresponding buffers by the master transceiver in accordance with the master channel bonding start information;

each of the slave transceivers operably coupled to:

receive the channel bonding sequence;

receive the channel bonding request and the channel bonding configuration information;

process the channel bonding request and the channel bonding sequence in accordance with the channel bonding configuration information to determine individual slave channel bonding start information; and

commence the channel bond writing of respective data to and reading of the respective data from corresponding buffers by the slave transceivers in accordance with the individual slave channel bonding start information.

29. The integrated circuit of claim 28, wherein the receiving the channel bonding sequence by the master transceiver further comprises:

receiving the channel bonding sequence within incoming data; and

detecting the channel bonding sequence within the incoming data.

30. The integrated circuit of claim 28, wherein the receiving the channel bonding sequence by each of the slave transceivers further comprises:

receiving the channel bonding sequence within incoming data; and

detecting the channel bonding sequence within the incoming data.

31. The integrated circuit of claim 28, wherein the receiving, by each of the slave transceivers, the channel bonding request and the channel bonding configuration

information further comprises:

receiving the channel bonding request and the channel bonding configuration information from the master transceiver; or

receiving the channel bonding request and the channel bonding configuration information from at least one intervening slave transceiver.

32. The integrated circuit of claim 28 further comprises the master transceiver generating the channel bonding configuration information further to include:

a number of slave transceivers;

propagation delays of each of the slave transceivers with respect to the master transceiver transmitting the channel bonding request; and

clock correction information.

33. The integrated circuit of claim 32, wherein the generating the clock correction information comprises:

generating pointer separation information;

generating an address offset; and

generating an adjust enable signal.

34. The integrated circuit of claim 33, wherein the generating the pointer separation comprises:

determining a read pointer of the master transceiver when the channel bonding sequence is received to produce a

master read pointer;

determining a write pointer of the master transceiver when the channel bonding sequence is received to produce a master write pointer; and

determining the pointer separation as a difference between the master read pointer and the master write pointer.

35. The integrated circuit of claim 33, wherein the generating the address offset comprises:

determining byte positioning of the channel bonding sequence with respect to a word line of memory of the master transceiver; and

establishing the address offset based on the byte positioning.

36. The integrated circuit of claim 33, wherein the processing, by each of the slave transceivers, the channel bonding request and the channel bonding sequence in accordance with the channel bonding configuration information to determine individual slave channel bonding start information comprises:

delaying the channel bonding sequence for a predetermined period of time based on the propagation delays of a corresponding one of the slave transceivers to produce a delayed channel bonding sequence;

determining whether receipt of the channel bonding request and the delayed channel bonding sequence are within a time window;

when the receipt of the channel bonding request and the delayed channel bonding sequence are within the time window:

determining a unique hold time based on a difference between the propagation delay of the corresponding one of the slave transceivers and a maximum propagation delay;

storing an address at which the channel bonding sequence was received by the corresponding one of the slave transceivers to produce a channel bonding sequence address;

determining a channel bonding write start address based on at least one of: the channel bonding sequence address, the channel bonding request, and the unique hold time; and

adjusting a read pointer and a write pointer of the corresponding one of the slave transceivers based on the pointer separation, the address offset, and the channel bonding write start address.

37. The integrated circuit of claim 36, wherein the determining whether receipt of the channel bonding request and the delayed channel bonding sequence are within the time window comprises:

when one of the delay channel bonding sequence or the channel bonding request is received, initiating the time window; and

determining whether the other one of the delay channel bonding sequence or the channel bonding request is received prior to expiration of the time window.

38. The integrated circuit of claim 36, wherein the adjusting the read pointer and the write pointer further comprises:

adding the address offset to the read pointer and to the write pointer.

39. The integrated circuit of claim 28, wherein the processing of the channel bonding sequence in accordance with the channel bonding configuration information and the channel bonding request to determine master channel bonding start information comprises:

storing an address at which the channel bonding sequence was received to produce a channel bonding sequence address; and

determining a channel bonding write start address based on the channel bonding sequence address and maximum propagation delay of the channel bonding configuration information.

40. A multi-gigabit transceiver comprises:
processing module; and

memory operably coupled to the processing module, wherein the memory stores operational instructions that cause the processing module to:

determine whether the multi-gigabit transceiver is a master transceiver or a slave transceiver;

when the multi-gigabit transceiver is the slave transceiver:

detect a channel bonding sequence at a given time to produce a detected channel bond sequence;

delay the detected channel bonding sequence for a predetermined period of time to produce a delayed channel bonding sequence;

receive a channel bonding request at a second given time;

determine whether the receiving of channel bonding request and the delayed channel bonding sequence are within a time window;

when the receiving of channel bonding request and the delayed channel bonding sequence are within the time window:

align data with respect to data alignment of the master transceiver to produce aligned data; and

synchronize the aligned data with data of the master transceiver.

41. The multi-gigabit transceiver of claim 40, wherein the memory further stores operational instructions that cause the processing module to determine whether the receiving of channel bonding request and the delayed channel bonding sequence are within the time window by:

determining whether the delayed channel bonding sequence occurs, in time, before the receiving of the channel bonding request;

when the delayed channel bonding sequence occurs before the receiving of the channel bonding request:

initiating a first clock cycle count from the delay channel bonding sequence to establish the time window;

determining whether the channel bonding request is received before expiration of the first clock cycle count; and

when the channel bonding request is received before expiration of the first clock cycle count, determining that the receiving of channel bonding request and the delayed channel bonding sequence are within the time window;

when the delayed channel bonding sequence occurs after the receiving of the channel bonding request:

initiating a second clock cycle count from the receiving of the channel bonding request to establish the time window;

determining whether the delayed channel bonding sequence occurs before expiration of the second clock cycle count; and

when the delayed channel bonding sequence occurs before expiration of the second clock cycle count, determining that the receiving of channel bonding request and the delayed channel bonding sequence are within the time window; and

when the delayed channel bonding sequence occurs at substantially the same time as the receiving of the

channel bonding request, determining that the receiving of channel bonding request and the delayed channel bonding sequence are within the time window.

42. The multi-gigabit transceiver of claim 40, wherein the memory further stores operational instructions that cause the processing module to align the data with respect to the data alignment of the master transceiver to produce the aligned data by:

determining a unique hold time based on a difference between propagation delay of the master transceiver detecting the channel bonding sequence and the slave transceiver receiving the channel bonding request and a maximum propagation delay;

storing an address at which the channel bonding sequence was received by the slave transceiver to produce a channel bonding sequence address; and

determining a channel bonding write start address based on at least one of: the channel bonding sequence address, the channel bonding request, and the unique hold time.

43. The multi-gigabit transceiver of claim 42, wherein the memory further stores operational instructions that cause the processing module to synchronize the aligned data by:

adjusting a read pointer and a write pointer of the slave transceiver based on pointer separation, an address offset, and the channel bonding write start address, wherein the pointer separation corresponds to a difference between a master read pointer and a master write pointer of the master transceiver and wherein the address offset

corresponds to byte positioning of the channel bonding sequence with respect to a word line of memory of the master transceiver.

44. The multi-gigabit transceiver of claim 40, wherein the memory further stores operational instructions that cause the processing module to, when the multi-gigabit transceiver is the master transceiver:

establish the predetermined period of time based on propagation delay between the master transceiver detecting the channel bonding sequence and the slave transceiver receiving the channel bonding request.

45. The multi-gigabit transceiver of claim 44, wherein the memory further stores operational instructions that cause the processing module to:

store an address at which the channel bonding sequence was received to produce a channel bonding sequence address; and

determine a channel bonding write start address based on the channel bonding sequence address and maximum propagation delay of channel bonding configuration information.